which is a ~32dB improvement from a standard ZC counting FDC running at $f_s$. However, due to noise assumed to originate from the signal generator itself, the measured SNR was found to be 56dB.

Norway (NFR) for financially supporting the project.

Fig. 5 Measured output spectrum for 271 Hz sinusoidally modulated FM input signal estimated by 21-point FFT, $D = 16$
Blackman data window

Fig. 6 Measured output spectrum for 271 Hz sinusoidally modulated FM input signal estimated by 21-point FFT, $D = 1000$
Blackman data window

Conclusion: We have shown that by introducing a triangular window in the traditional ZC counting FDC, $\Delta\Sigma$ noise-shaping and decimation result. A simple way to implement the windowing function is by using a double modulo counter or sinc$^2$ decimator. In this way, using a $\Delta\Sigma$ decimator as a ZC counting FDC, a higher digital resolution can be achieved than by using a standard count-and-dump FDC, as the quantisation error is noise-shaped.

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Wide and continuously tunable (30nm) detector with uniform characteristics over tuning range

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Indexing terms: Micromechanical devices, Wavelength division multiplexing, Detector circuits

A wide and continuously tunable detector with a tuning range of 30nm ($\Delta\lambda = 3.7\%$) is demonstrated. Uniform responsivity of $-0.13\Omega$/W and a linewidth of ~5nm is achieved over the tuning range. This device is well suited for both single and multimode, dense and sparse channel separation WDM applications.

Wavelength division multiplexed (WDM) applications are rapidly expanding not only in long-haul but also in multimode local area network applications in the 830/850nm wavelength regime [1, 2]. For multimode WDM applications, the channel spacing is required to be much wider at 10-15nm, due to the broad spectra of multimode lasers. Thus, the key components required are widely and continuously tunable, cost-effective lasers and detectors. While there are many approaches for tunable lasers, there has been little work on compact continuously tunable detectors and those available [3] are limited in tuning range to a few nanometres and the structure does not merit cost-effective manufacturing.

Of all the tuning mechanisms, mechanically changing the effective length of a Fabry-Perot tuning cavity offers the largest continuous tuning range [4 - 7]. We have previously demonstrated a resonant-cavity detector (RCD) with a micromechanically tuned vertical cavity [4]. Although exhibiting a reasonable tuning range, the responsivity and linewidth were highly nonuniform over the whole tuning range. This is because the tunable airgap was a part of the top of the distributed Bragg reflector (DBR) of the RCD, the reflectivity of which changes slightly as the cantilever tunes. The responsivity and linewidth of an RCD, however, requires a careful balance of mirror reflectivities and detector absorption region position [8]. Thus, as the cantilever tunes, the characteristics exhibits a tuning-dependence, which severely limited the usable bandwidth of the device.

Fig. 4 Schematic diagram of tunable detector showing freely suspended cantilever

Device is essentially a tunable filter with monolithically integrated detector. Detector bias is controlled by $V_{det}$, while cantilever tuning is determined by $V_{bias}$.
In this work, we circumvent the intrinsic weakness of a tunable RCD by placing the integrated detector beneath a tunable filter. We achieved 30 nm continuous tuning ($\Delta \lambda = 3.7\%$), from 824 to 794 nm. Uniform peak responsivity of $0.13\, A/W$ and a constant linewidth of $\approx 5$ nm is achieved with this device over the tuning range. The device has a surface normal geometry, which facilitates both single and multimode fibre coupling and integration with other components.

A schematic diagram of our tunable detector is shown in Fig. 1. The 20 x 20 μm filter is formed with 1.9 air-gap cavity (~0.9 μm) sandwiched between a moveable top mirror supported by a 4 x 100 μm freely suspended cantilever and a fixed bottom mirror. The top mirror is a 13-pair n-doped Al$_x$Ga$_{1-x}$As-Al$_y$Ga$_{1-y}$As DBR and the bottom mirror is an 18-pair p-doped Al$_x$Ga$_{1-x}$As-Al$_y$Ga$_{1-y}$As DBR. The calculated reflectivity of both DBRs is 98%. The absorption region is a 1.2 μm GaAs layer (~450 μm), directly beneath the filter. The air-gap thickness and the Fabry-Perot wavelength can be changed by electrostatically actuating the top DBR with a voltage. The incoming signal is focused onto the top of the cantilever head, filtered through the Fabry-Perot cavity and is then absorbed by the reverse biased detector underneath. The whole structure is grown by molecular beam epitaxy (MBE). Device fabrication is extremely simple, consisting of three non-critical lithography steps with self-aligned processes.

![Fig. 2 Typical detector responsivity against wavelength for different applied tuning voltage](image)

30 nm of continuous tuning is demonstrated with 7.6 V tuning voltage.

![Fig. 3 Typical detector responsivity lineshape in both linear and log scale](image)

- a Linear
- b Log scale

Lorentzian lineshape is obtained.

High extinction ratio of 15 dB is achieved.

~5 nm FWHM is very suitable for multimode fibre applications.

The tuning characteristics of a typical device are shown in Fig. 2. The device tuned from 824 to 794 nm with 7.6 V, resulting in 30 nm continuous tuning. This tuning range is limited by our characterisation setup (limited by the tunable Ti:sapphire laser, which stops lasers below 780 nm). A tuning range as large as 70 nm is theoretically achievable [3]. A peak responsivity of 0.13 A/W is obtained. This is mainly limited by the ~8.7 dB insertion loss of the filter, which is calculated by comparing the overall detector responsivity with that of the GaAs absorption layer only. This relatively high insertion loss is mainly due to a ~3% growth rate drift error during the MBE growth. This can be easily corrected for with a better calibrated growth.

![Fig. 4 Typical detector peak responsivity and lineshape FWHM against wavelength over entire tuning range](image)

Average peak responsivity of 0.13 A/W with standard deviation of 0.016 A/W is obtained over entire tuning range. Average lineshape FWHM of 5 nm with standard deviation of 0.6 nm is also achieved over 20 nm of tuning.

Peak responsivity and lineshape full-width-half-maximum (FWHM) against tuning wavelength are shown in Fig. 4. An average peak responsivity of 0.13 A/W with a standard deviation of 0.016 A/W is obtained over the entire tuning range. An average lineshape FWHM of 5 nm with a standard deviation of 0.6 nm is also obtained over 20 nm of tuning.

In conclusion, we have demonstrated a wide and continuously tunable detector with uniform peak responsivity and a linewidth over a 30 nm tuning range. The uniform tuning characteristic is a result of our new design, by placing the detector out of the resonant cavity. It is essential to point out that all the parameters can be designed and optimised. This tunable detector design is very suitable for both singlemode and multimode fibre and dense and sparse WDM applications. Furthermore, the design principle can be readily transferred to the 1.3–1.5 μm regime with the appropriate choice of material.

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References

Bit-serial interleaved high speed division

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Indexing terms: VLSI, Dividing circuits

A bit-serial/word-parallel divider circuit with simplified control requirements is presented. The circuit uses the non-restoring division algorithm which places a restriction on the speed of the circuit. By introducing the concept of bit interleaving, a high speed design can be implemented of the same circuit complexity as an equivalent size multiplier.

Introduction: The nature of the division algorithm is such that quotient bits are computed MSB-first, unlike multiplication where first and MSB-first multipliers have been proposed [7] for use with the product bits are formed LSB-first. The arrays presented in these converters. In this Letter, a high speed bit-serial divider circuit with low control complexity using an MSB-first approach is presented.

Bit-serial division: When dividing a word d of n bits (the dividend) by a word c of m bits (the divisor), the result of the division (or quotient) y has a word length of \( n+m-1 \):

\[
y = \frac{d}{c} = d_{n-1}d_{n-2}\cdots d_0 + \frac{d_{n-1}}{c_{m-1}}c_{m-2} + \cdots + \frac{d_0}{c_0}c_{m-1}c_{m-2}\cdots c_0 = y_{n-1}y_{n-2}\cdots y_0 y_{-m}
\]

It is assumed in the evaluation of \( d/c \) that \( |c| > |d|, c \neq 0 \) and the numbers are in two’s complement form with sign bits \( c_0 \) and \( d_0 \). Either restoring or nonrestoring division can be used to implement the division algorithm on cellular arrays. Restoring division requires two operations per cycle, but nonrestoring division is the preferred algorithm since it requires a single operation (addition or subtraction) per cycle. In nonrestoring division, the operation to determine bit \( y_0 \) of the quotient is dependent on the result \( y_{-1} \) derived from a carry out signal \( c_r \). The addition or subtraction of the divisor to or from a partial remainder (PR) is chosen such that the current partial remainder is reduced towards zero [1 – 3]. In the case of a negative divisor, the output must be negated to obtain the correct quotient. The algorithm for positive division and negative divisor, illustrated in Fig. 1, produces MSB (\( y_n \)) first. The XOR operation is used to produce a one’s complement quotient, given \( c_0 = 1 \), resulting in an error of \( 2^{m-1} \).

MSR first division array: The bit-serial/word-parallel array in Fig. 2 implements the nonrestoring division algorithm using \( m \) simple processing elements of a controlled-add-subtract (CAS) cell. The divisor \( c \) is presented in parallel with the dividend \( d \) entered into the array in a bit-serial manner, MSB \( d_{n-1} \)-first. An initialisation phase of \( m-1 \) clock cycles is required to enter the \( m \) most significant bits of \( d \) into the array. During this phase, the control signal \( lD \) is held at zero such that the parallel values \( c \) and the carry in signal are disabled. During the following \( n-m+1 \) clock cycles, the quotient \( y \) is produced MSB-first. The operation of the first cycle is determined by \( c_0 \) and \( d_0 \) with subsequent cycles determined by \( c_r \) and the carry out of the right hand cell \( c_r \). Thus, another control line \( msh \), to identify cycle \( m-1 \), is required.

![Fig. 1 Non-restoring division for negative divisor and positive/negative dividend, with \( n = 7 \) and \( m = 4 \)]

Note error due to one’s complement calculation of quotient in this case

Pipelined array: The long combinational path of the carry in Fig. 2 prohibits high speed operation. Pipelining the carry results in the insertion of an extra \( m+1 \) flip-flops on each of the partial product lines between processing elements, as illustrated in Fig. 3 where \( K = m+2 \). The latency of this circuit increases to \( m(m+1) \) clock cycles, with \( m+1 \) clock cycles between each bit \( y_r \).

![Fig. 2 Non-restoring bit-serial divider]

(a) Linear array of \( m \) cells
(b) Key to full adder

![Fig. 3 Pipelined bit-serial divider]

\( msh \)