III-V Nanopillar Phototransistor Directly Grown on Silicon

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Abstract: We demonstrate InP nanopillar bipolar junction phototransistors monolithically integrated on a Silicon substrate. With a responsivity of 4 A/W and bandwidth of 7.5 GHz, these receivers indicate a route towards efficient on-chip optical interconnects.

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1. Introduction: seamless optoelectronic integration

Optical interconnects are inherently free of the resistive-capacitive physics that dominates delay and energy consumption in electrical wires – but instead require highly efficient and low energy components in order to be a compelling alternative at the shortest length scales. A benchmark for comparison would be that electrical links are not expected to scale below 110 aF/µm capacitance per unit length[1], which decides the charging energy of these wires. Thus, optical links become compelling at lower and lower length scales as the photodetector capacitance shrinks. An ultralow capacitance receiver enables low optical link power since it allows a minimal number of photons to actuate logic level voltage swings. III-V materials integrated on a Silicon substrate are very promising for efficient low capacitance receivers due to their high absorption coefficient.

Given that a wavelength-scale volume of semiconductor has a capacitance on the order of 100-200 aF at minimum, it is expected that the most energy efficient optical links, with drastically reduced link power, will additionally still require some form of gain or amplification circuitry to drive electronics. It is then necessary that the receiver amplifier circuit be intimately integrated with the photodetector – else the 110 aF/µm capacitance of the wire to the receiver will overwhelm any benefits of having a miniaturized detector[2]. In this work, we have used the technology of catalyst-free III-V nanopillar integration on Silicon[3] to demonstrate InP-based p-n-p bipolar junction phototransistors. These devices detect incident light efficiently within a micrometer-scale volume and also show fast transistor action with the photovoltage actuating the BJT in active mode operation. The high absorption of the material could potentially allow a scaling of the detector capacitance down from 1-10 fF to the 100 aF regime. To the best of our knowledge, this is the first experimental demonstration of a monolithically integrated III-V based optoelectronic receiver on Silicon.

2. Growth and Fabrication: epitaxial regrowth technique

The nanopillar devices are grown in a MOCVD reactor under CMOS back end of line integration compatible conditions. In particular, the growth temperature is around 450 °C and no gold catalyst is used to nucleate the nanopillar growth. The growth is naturally in a core shell mode, with time-scaling pillar size, free of lattice-matching constraints. Spatially precise impurity doping can be achieved by the in-situ introduction of dopant precursors during MOCVD growth. When light is incident on the pillars, the generation of carriers leads to a Fermi-level split. Or equivalently, a photovoltage is created in the pillar, depending on the input photon current I_{ph}, non-radiative recombination or dark current I_d and the thermal voltage kT/q:

\[ V_{ph} \sim \frac{kT}{q} \ln \left( \frac{I_{ph}}{I_d} + 1 \right) \]  

(1)

This photovoltage, if generated in the base region of the structure, leads to transistor action by reducing the potential barrier to carrier flow in the p-n-p device (Fig. 1a). But, in order to obtain a sufficiently high voltage with realistic optical power, the dark current needs to be low. With a core-shell structure, the outer shell layers will be shunted to the substrate, leading to a high dark current. A regrowth technique was implemented, whereby the p-core of the BJT structure was grown first. The sample was then removed from the MOCVD chamber, and a dielectric layer was coated on it, with openings defined on the upper portion of the pillars. The sample was then regrown through MOCVD such that the shell only grew on the upper exposed portion of the pillar – with the dielectric mask preventing the formation of a shunt path. This process was crucial to the formation of non-shunted devices that showed transistor action. Figure 1b shows the final structure of the device with the regrown section defined only on the upper portion of the nanopillar.
Figure 1: Schematic and DC measurements of the nanopillar phototransistor. (a) The two-terminal phototransistor uses the band bending from the photogenerated carriers (blue) to lead to transistor action. (b) Schematic showing the layer structure of the device, with the p-n-p layers defined on the upper exposed section of the p-core using the regrowth technique, W(base width) ~ 50 nm, L ~ 4 μm. (c) 30 degree tilt view SEM image of the pillar, showing the gold contact with angled metal evaporation. (d) Forward active operation of the two terminal device, with 785 nm laser light incident on the uncoated side of the pillar. (e) Photocurrent vs. incident optical power, showing a responsivity of 4 A/W, and a linear characteristic at V_{ce} = 0.6 V.

3. DC and high speed measurements

High speed ground-signal contacts were defined via lithography on individual nanopillars to measure both DC and AC responses. Angled evaporation of gold was carried out to allow light access for optical characterization. Fig. 1b shows an SEM image of the device. Pulsed optical characterization was carried out with a tunable Ti:sapphire femtosecond laser tuned to 785 nm, with a repetition rate of 80 MHz and pulse width of ~100 fs. The high speed collector current response was measured using an oscilloscope (Fig. 2a) and Fourier transformed to obtain the device bandwidth. The 100 μm large contact pads limited the frequency response, and were calibrated out with a network analyzer, using a standard S_{11} measurement. After de-embedding the pad parasitics, the 3 dB bandwidth of the device was calculated to be 7.5 GHz.

In conclusion, we have demonstrated a sensitive, high-speed phototransistor – which is a novel receiver design with a seamless integration of detection and receiver circuit. Connecting and coupling efficient III-V nanopillar-based components could truly enable short distance optical links.

4. References