EE C235 / NSE C203 – Nanoscale Fabrication (Spring 2009)
Prof. Connie Chang-Hasnain
Homework 1
Due date: 03/02/09, by 2:40pm in class

Problem 1 – Density of States:

We have derived the 3D, 2D, 1D and 0D density of states (DOS) in the class. Please answer the following questions. You may also use this online reference.
http://ece-www.colorado.edu/~bart/book/book/chapter2/ch2_4.htm#2_4_2

(a)

Plot the 3D and 2D DOS versus energy E. You do not have to re-derive the equations but please write down the equations you use for your plots. Suppose that the confinement is in the z-direction for the 2D case, i.e., L_z is small while L_x and L_y are large.

(b)

Suppose we are looking at the conduction band so there are only electrons. On the 3D and 2D DOS plot, **graphically show** which area is proportional to the electron concentration for the 3D and 2D case, respectively, and **explain why**. Assume that T= 0K and the Fermi-energy E_F lies between the 1st and the 2nd quantized energy levels of the 2D structure.

(c)

Fact 1: The "gain curve" (gain versus energy E) of a laser is (to some degree) proportional to the DOS. **Fact 2:** The injection current of a laser is proportional to the number of the injected electrons that we just calculated in (b).

For a laser to "lase", we have to inject enough electrons into the conduction band to let the gain reach the threshold condition g_{th}. Based on these facts and your 3D and 2D DOS plots, **please explain** (e.g., from the injection current consideration) why people prefer to use quantum well structures for a laser diode instead of a bulk material?

(d)

Hand-plot the 1D DOS. This is the nanowire case. Assume that the confinement occurs at the x and y directions. L_x and L_y are small while L_z is large. Also assume that $L_x = L_y$ (This will result in some degeneracy in energy levels.).

(e)

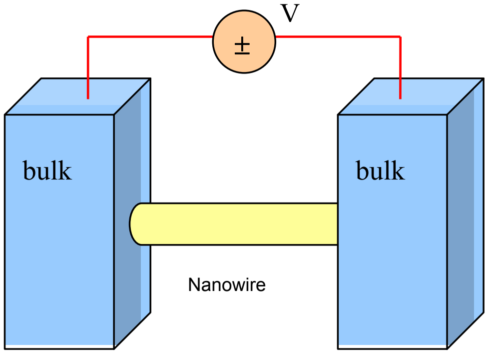
Hand-plot the 0D DOS. This is the quantum dot (or quantum box) case. Assume that $L_x = L_y = L_z$ and they are all very small. (Again there will be some degeneracy in energy levels. Be careful.).

(f)

Quantum dot lasers have superior wavelength stability against the environmental temperature fluctuation. Please use the DOS to explain this.

Problem 2 – Nanowire conductance:

Consider a nanowire with diameter *d* and length *L*. Let it be bridged between two bulk regions of the same material. Bulk means no quantization of any kind. We applied a voltage between the two bulk regions.



(a)

Derive and sketch the conductance as a function of voltage of this junction. Label important features. [Hint: conductance will be quantized.]

These references will be helpful:

http://en.wikipedia.org/wiki/Ballistic_transport

http://128.200.94.85/Nano04/Lectures/Lecture10Notes.pdf

http://128.200.94.85/EECS217C/Lectures/Lecture11forweb.pdf

(b)

Sketch the current-voltage characteristics. Label important features.

Problem 3 – Solar Cell:

We are going to design a traditional p-n junction Si solar cell. The current I of an ideal p-n diode is related to its bias voltage V as $I=I_0(e^{qv/kT}-1)$, where I_0 is a constant called reverse saturation current, q is the single electron charge, k is Boltzmann constant and T is the temperature. The definition of the "positive" current direction here is from p-side to n-side. When this p-n junction is under illumination, there will be photo current I_L.

The direction of I_L is from n-side to p-side due to the direction of the p-n junction built-in voltage. Therefore, according to the previous definition of "positive" current direction, the total current when there is illumination is $I' = I_0(e^{qv/kT}-1)-I_L$.

A little bit more on I_0 and I_L. $I_0=qA[D_e n_i^2/(L_e N_A)+D_h n_i^2/(L_h N_D)]$ and $I_L=qAG(L_e+W+L_h)$. A is the cross section area of the diode, n_i is the intrinsic carrier concentration, G is the carrier generation rate under illumination, N_A is the doping concentration in the p-type region (hence is also the hole concentration in the p-region), N_D is the doping concentration in the n-type region (hence is also the electron concentration in the n-region). Holes in the p-region and electrons in the n-type are all majority carriers. D_e is the electron diffusion constant in the p-type region, L_e is the electron diffusion length in the p-type region. Electrons in the p-region are minority carriers (their concentration is much less than the hole concentration there). D_h is the hole diffusion constant in the n-type region, L_h is the hole diffusion length in the n-type region. Again holes in the n-region are minority carriers. W is the width of the depletion region. L_e and L_h give an estimate of how far an minority carrier can survive from the edge of the depletion region. For more details on a p-n junction, including how all the above equations are derived, please check this wonderful online reference.
http://ece-www.colorado.edu/~bart/book/book/chapter4/ch4_1.htm

(a)
Plot I-V curves for both the dark and illuminated conditions.
(b)
The illuminated case is actually a solar cell. Please derive the open-circuit voltage V_{oc} as a function of I_0, I_L and other necessary parameters.
(c)
Give some physical explanations of why I_L is as shown above.
(d)
Given $T = 300\ K$, $N_A = 10^{18}\ cm^{-3}$, $N_D = 10^{15}\ cm^{-3}$, $A = 1\ cm^2$, $G = 10^{19}/s\text{-}cm^3$, **estimate V_{oc}**. Assume room temperature operation. [Hint: W is typically much less than L_e and L_h so you may neglect W when calculating I_L. Apply proper values for D_e, D_h, L_e, L_h, n_i to find out V_{oc}. You can find all the parameters from the link below.
Another equation you might need to use: $L_h=(D_h\tau_h)^{1/2}$, where τ_h is the minority carrier life time of hole in the n-type region. A similar equation applies to the electrons in the p-type region.]
http://www.ioffe.rssi.ru/SVA/NSM/Semicond/Si/electric.html

Problem 4 - VCSEL:

Unlike the Si-based processes, laser devices, which use compound semiconductors, generally require thin film epitaxy as the first step. Suppose that you are given an epitaxy wafer as shown in Fig. 1. Please design a process flow to fabricate a VCSEL device as shown in Fig. 2. The following process conditions and constraints are to be considered.

(i) The metallization process (contact formation) actually consists of two processes. The first is the metal deposition and then followed by proper annealing to make the metal-semiconductor contact ohmic. Assume here the p-type metal annealing condition is 420 °C for 3 minutes in a rapid thermal annealing (RTA) equipment. The n-type metal annealing condition is 380 °C for 3 minutes. Over annealing (temperature too high) generally will result in a deleterious effect to the metal-semiconductor contact resistance.

(ii) The oxidation process is to convert part of the AlAs layer into aluminum oxide, which is an insulator that blocks the current flow. The purpose is to let the current flow through only the central $\sim 5\mu$m cylindrical region of the device to control the laterallasing modes. Assume the oxidation process is done in a furnace with water vapor supply at 450 °C for 30 minutes.

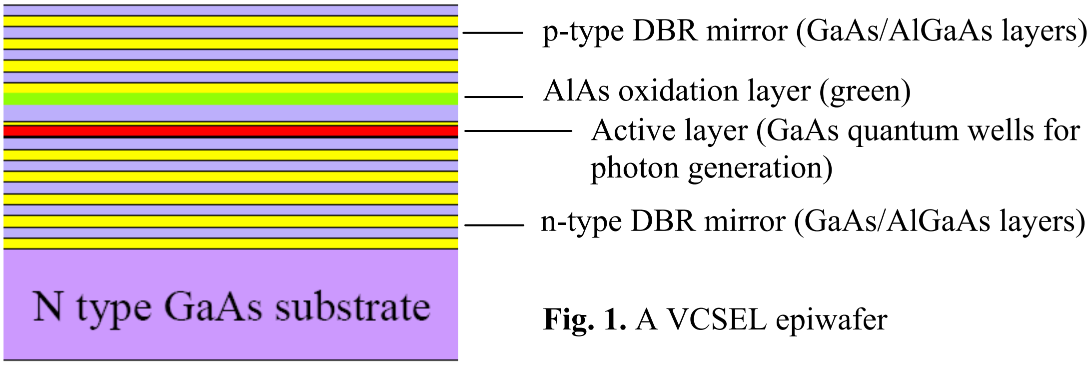


Fig. 1. A VCSEL epiwafer

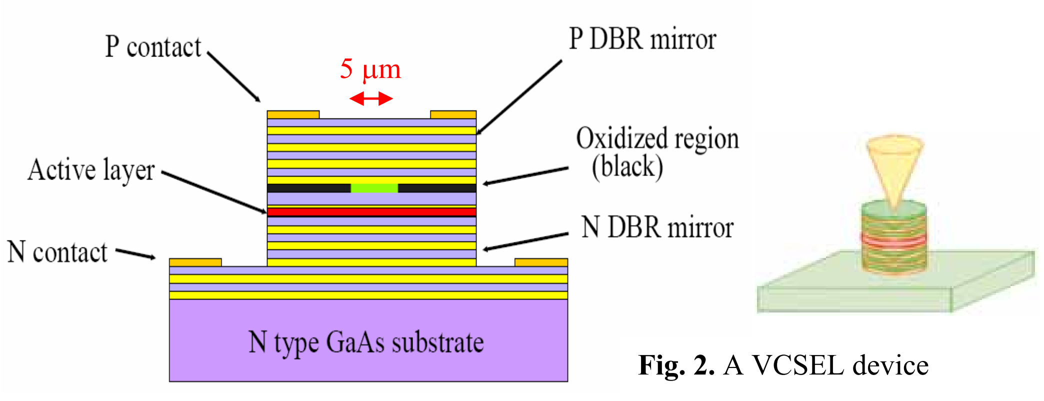


Fig. 2. A VCSEL device

(a)

Please design a process flow, which might result in the best device performance. Please specify each lithography step like those shown in the applets in Problem 1 and 2. Please also draw the top views of all the masks used. (There are NOT too many steps here so don't worry!)

(b) When etching a VCSEL "pillar", either dry etching or wet etching could be used. Please compare the pros and cons of these two methods.